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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,382	02/16/2000	Roy R. Faget	10001840-1	6474

22879 7590 03/25/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	23

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/505,382	FAGET, ROY R.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment D, filed 2/4/2004.

2. Claims 1-20 are pending in this application. Claims 1 and 11 are independent claims. In Amendment D, claims 1 and 11 are amended. This action is made non-final after a filed Request for Continued Examination.

Claim Objections

3. Claims 5 and 15 are objected to because of the following informalities:

Re claim 5, it has limitation that is already cited in the amended claim 1 lines 13-14.

Re claim 15, it has same problem as cited in claim 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 8-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being obvious over Vatinel (U.S. 6,317,763) in view of Potter et al. (U.S. 6,324,239).

Re claim 1, Vatinel discloses a logic circuit in Figure 1 for use in a multiplexer to shift the input data (col.. 1 lines 19-22) comprising: a plurality of logic gates (nine rows wherein each row comprising transistors), each logic gate receiving data input (upper portion of 6 and col. 1 lines 29-31) and control signals (lower portion of 6 and col. 1 lines 37-39) wherein each data input line has a one to one correlation to a single data transistor (each input data is connecting to a buffer as seen in part 6 of Figure 1 wherein the buffer is inherently comprised transistors but has only one transistor interfaces with the input data line); and wherein the control signals include a plurality of control lines to provide for multiple shifting operations (Figure 2 part 30 and Figure 1 part 7 wherein there are two control signals go 7 into each array of transistors 8); and a plurality of shared data lines (the data bus from outputs of the buffers to all plurality of logic gates) connecting logic gates the shared data lines providing a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates (e.g the second input data is connected to an buffer and the output of buffer is connected to all other logic gates across the array), wherein the logic gates shift data received at the data inputs based upon the control signals (col. 1 lines 42-44) and the connections of the shared data lines to produce a shifted data output (output data 5), and wherein all of the plurality of logic gates share a single data transistor for each data input (all the parts of row logic gates is are connected to the output of input data buffer) wherein each of the logic gates receives one data input using the single data transistor and receives other data inputs from adjacent logic gates using the plurality of shared data lines to reduce the number of data transistors required (only the front transistor in Figure 1 receive the input signal directly wherein

other sub-transistors receive signal from neighborhood). Vatinel does not disclose the logic gates are dual rail Domino. However, dual rail Domino is well known in the art as seen in Potter et al.'s Figure 1. Potter et al. disclose the dual rail Domino logic gates in shifter (col. 2 lines 1-14). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the dual rail Domino logic gates as seen in Potter et al.'s invention into Vatinel's invention because it would enable to increase the stability and flexibility of system.

Re claim 2, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates includes first (shift) and second (un-shift) stages shift operation.

Re claim 3, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates includes control inputs for receiving two set of shift control signals (the control signal 7 is inputted into the logic gates by 4) for the first and second stages of shifting.

Re claim 4, Vatinel further discloses the above logic circuit comprising another plurality of shared data lines (data bus from output of buffers 6 to rows of logic gates 8) for providing data inputs to the second stage of shifting for the second shifting operation.

Re claim 5, Vatinel further discloses the above logic circuit in Figure 1 wherein the plurality of shared data lines connect adjacent logic gates (the shared data bus connect all the parts of row of logic gates as a step) among the plurality of logic gates.

Re claim 6, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates receives as one of the data inputs (input data 6) as a primary data line.

Re claim 8, Vatinel further disclose the above logic circuit in Figure 1 wherein each of the logic gates control by the control signals (4) and the logic gates including a plurality of transistors (8).

Re claim 9, it has similar limitation cited in claim 1. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 10, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the shared data lines connect one of the logic gates with a plurality of the logic gates (in Figure 1, the share data bus from input data buffer connects all the plurality of the logic gates together at different parts).

Re claim 11, it is a method claim of claim 1. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 12, it is a method claim of claim 2. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 13, it is a method claim of claim 3. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 14, it is a method claim of claim 4. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 15, it is a method claim of claim 5. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 16, it is a method claim of claim 6. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 8. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 19, it is a method claim of claim 9. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 20, it is a method claim of claim 10. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 10.

6. Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Vatinel (U.S. 6,317,763) in view of Potter et al. (U.S. 6,324,239), as applied to claims 1 and 11 respectively, in further view of Hervin et al. (U.S. 5,961,575).

Re claim 7, Vatinel in view of Potter et al. do not disclose each of the logic gates receives a clocking signal for enabling the logic gates to feed data. However, Hervin et al. disclose in Figure 3 a system clock is used to trigger the data for inputting and shifting. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a clock signal as seen in Hervin et al.'s invention into Vatinel in view of Potter et al.'s Figure 1 because it would enable all the data synchronize properly for shifting (Figure 3).

Re claim 17, it is a method claim of claim 7. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 7.

Response to Arguments

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

8. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Vatinel does not disclose or suggest the feature of enabling all of the logic gates to share a single data transistor for each data input) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

March 18, 2004

TODD INGBERG
PRIMARY EXAMINER